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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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10/655,363

09/04/2003

John G. Edelen

2001-0886.01

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12/27/2004

LEXMARK INTERNATIONAL, INC.
INTELLECTUAL PROPERTY LAW DEPARTMENT
740 WEST NEW CIRCLE ROAD
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LEXINGTON, KY 40550-0999

EXAMINER

DUDDING, ALFRED E

ART UNIT

PAPER NUMBER

2853

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/655,363

Applicant(s)

EDELLEN ET AL.

Examiner

Alfred E. Dudding

Art Unit

2853

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>1/22/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 10, 14, 16, 25, and 29 – 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carrigan, III (U.S. 6,546,177 B1 in view of Conta et al. (U.S. 6,371,589 B1).

Carrigan, III discloses an inkjet printhead, Figure 1B, element 116, and a method of controlling the temperature of a printhead (Figure 28); resistor elements to heat the printhead, Column 35, lines 20 – 31, Figure 31, element 3115; a controller of the resistor elements, Figure 1B, element 124, and temperature sensors operatively connected to the controller to enable the controller to monitor the chip temperature the resistors elements to heat the chip.

Carrigan, III fails to teach the claimed inventions of MOS logic blocks on the printhead chip and that the temperature sensors are resistors implanted on the chip.

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Conta et al. disclose that the printhead chip consists of MOS logic blocks, Column 1, lines 53 – 60; that the temperature sensor is an implanted resistor (TSR) made using CMOS techniques, and that the printhead may contain hundreds of nozzles and associated sensors, Column 2, lines 14 – 46.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CMOS logic blocks and implanted TSR of Conta et al. in the printer and printhead of Carrigan, III in order to integrate several components of a printhead using fewer manufacturing steps by using CMOS techniques thereby reducing power consumed and also giving a smaller chip footprint.

4. Claims 2 – 9, 11 - 13, 15, 17 – 24, and 26 - 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carrigan, III in view of Conta et al. as applied to claims 1 and 16 above, and further in view of Tanaka et al. (U.S. 2002/0060333 A1), Aswell (U.S. 2001/0050410 A1, and Stanley Wolf, Silicon Processing for the VLSI Era, Volume 2, Lattice Press, 1990, pp.354-356.

The combination of Carrigan, III and Conta et al. fail to teach the claimed invention of a TSR having a sheet resistance of at least 1000 ohms/square and a temperature coefficient of resistance (TCR) of at least 0.0040 ohms/degree C.

Tanaka et al. disclose an implanted resistor made of N-well material and having a sheet resistance of 1000 ohms/square, paragraph [0049]. Tanaka et al. fails to teach the claimed invention of a TCR of at least 0.0040 ohms/degree C.

Aswell discloses that the TCR may range from 600 to 6000 ohms/degree C, (0.0006 to 0.0060 ohms/degree C), paragraph [0038] and that the thickness of the resistor is 1 μm ,

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paragraph [0007]. The length and width of the resistors depends on the sheet resistance and would be obtained with the formula of paragraph [0005]; if one dimension is chosen, the other is thereby obtained, making the resistor footprint a matter of design choice.

Stanley Wolf discloses lightly doped drains (LDD) in making CMOS devices using PSD and NSD material, Table 5.2, p. 355. Given Carrigan, III and Conta et al. teachings of CMOS technology, LDD would have been used for its known function of their channel effects.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use material having the sheet resistance of Tanaka et al., the TCR of Aswell, and the materials of Stanley Wolf to make the implanted TSR of Carrigan, III and Conta et al. in order to obtain a TSR having a resistance variation of a magnitude to be detectable above the noise level of the printhead chip yet being small enough to be associated with each nozzle of the printhead.

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Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alfred Dudding whose telephone number is (571) 272-2144. The examiner can normally be reached on Monday-Friday from 7:00 AM to 3:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Meier, AU 2853, can be reached at (571) 272 - 2149. The fax phone number for this Group is are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

Alfred Dudding

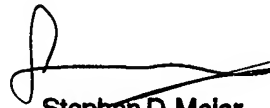
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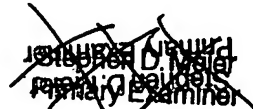
Art Unit: 2853

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Stephen D. Meier
Primary Examiner

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Stephen D. Meier
Primary Examiner~~

Alfred Dudding



16 December 2004